Issue Date:Oct.19.2007
Model No.: V420B1-LH1

Approval

TFT LCD Approval Specification

MODEL NO.: V420B1 - LH1

Customer: _____

Approved by:_____

Note:

Approved By	TV Head Division	
	LY Chen	

Reviewed By	QRA Dept.	Product Development Div.
	Tomy Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver.1.0	Mar.08,'07	All	All	Preliminary Specification was first issued.
Ver.2.0	Oct.19,'07	All	All	Approval Specification was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420B1-LH1 is a 42" TFT Liquid Crystal Display module with 16-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1366 x 768 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (1500:1)
- Dynamic contrast ratio (6000:1)
- Fast response time (Gray to gray average 4.0 ms)
- High color saturation (NTSC 72%)
- HDTV (1366 x 768 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 100/120 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- 180 degree rotation display option
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.246(H) x 523.008 (V) (42.02" diagonal)	mm	(1)
Bezel Opening Area	939 (H) x 531 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch(Sub Pixel)	0.227 (H) x 0.681 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

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1.5 MECHANICAL SPECIFICATIONS

	Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	982.0	983.0	984.0	mm	(1), (2)
	Vertical (V)	575.0	576.0	577.0	mm	
	Depth (D)	53.5	54.5	55.5	mm	
Weight		12300	12500	12700	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta $\leq$ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

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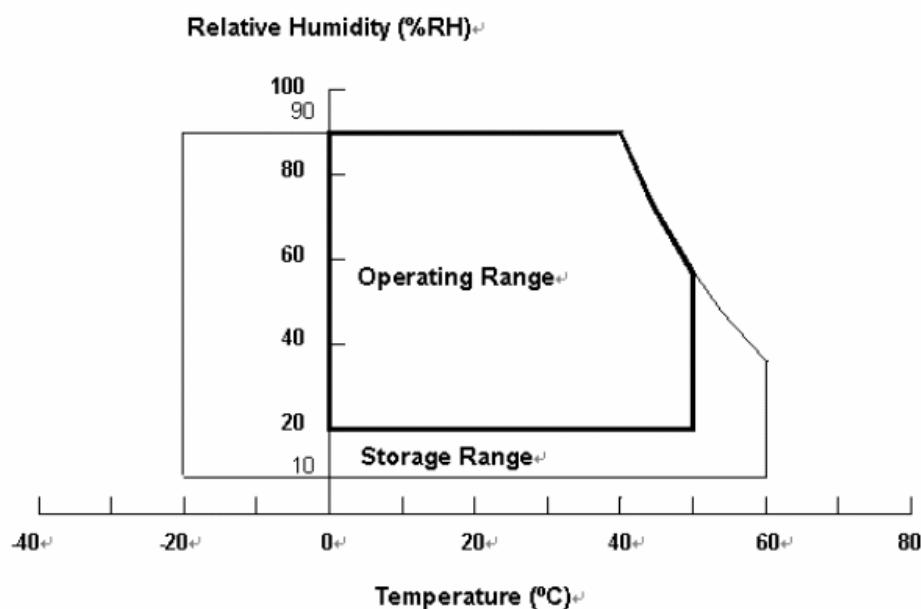
2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	—	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation

should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

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3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	10.8	12	13.2	V	(1)
Power Supply Ripple Voltage		VRP	-	-	250	mV	
Rush Current		IRUSH	-	-	4.5	A	(2)
Power Supply Current	White	- - -	-	1.48	1.70	A	(3)
	Black		-	0.66	-	A	
	Vertical Stripe		-	1.33	-	A	
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	-	-	100	mV	
	Differential Input Low Threshold Voltage	VLVTL	-100	-	-	mV	
	Common Input Voltage	VLVC	1.125	1.25	1.375	V	
	Terminating Resistor	RT	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

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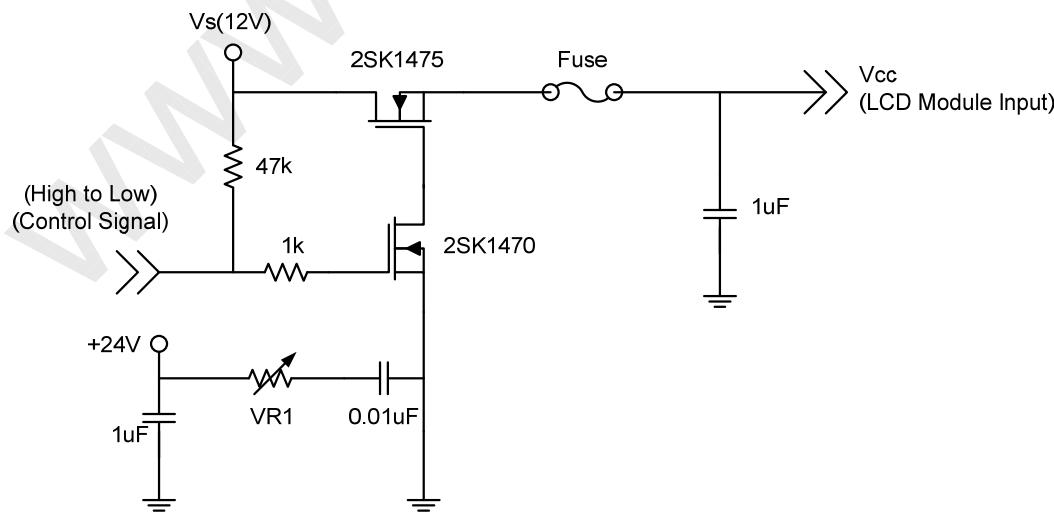
Vcc rising time is 470us
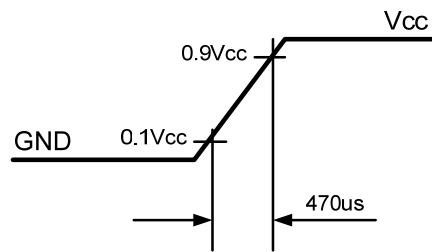
Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, fv = 120 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern
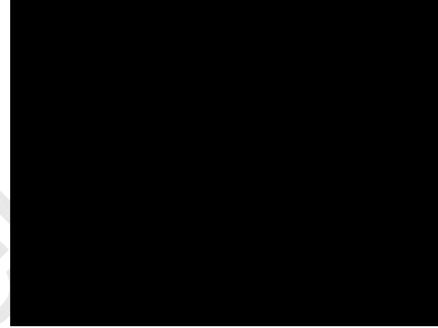
Active Area

c. Vertical Stripe Pattern

Active Area

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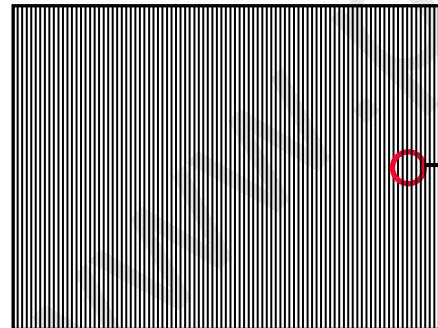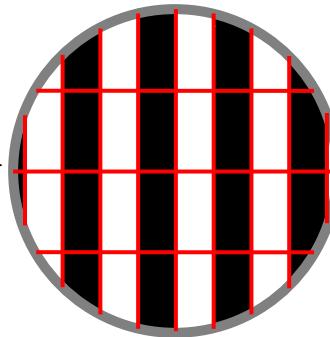
3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	VL	-	1490	-	VRMS	-
Lamp Current	IL	6.0	6.5	7.0	mARMS	(1)
Lamp Turn On Voltage	VS	-	-	2370	VRMS	Ta = 0 ºC (2)
		-	-	2160	VRMS	Ta = 25 ºC (2)
Operating Frequency	FL	40	-	70	KHz	
Lamp Life Time	LBL	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption at Gray level 255	P255	-	150	160	W	(5)(6), IL =6.8mA
Power Consumption at Gray level 128	P128	-	75	-	W	Dynamic BLU Enable
Power Consumption at Gray level 0	P0	-	50	-	W	Dynamic BLU Enable
Power Supply Voltage	VBL	22.8	24	25.2	VDC	
Power Supply Current	IBL	-	6.25	-	A	Non Dimming
Input Inrush Current	-	-	-	9.8	Apeak	
Input Ripple Noise	-	-	-	912	mVP-P	VBL=22.8V
Oscillating Frequency	FW	47	50	53	kHz	(3)
Dimming frequency	FB	150	160	170	Hz	
Minimum Duty Ratio	DMIN	-	20	-	%	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

Note (2) The lamp starting voltage VS should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the

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effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and IL =6.0~7.0mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 42" backlight unit under input voltage 24V, average lamp current 6.8 mA and lighting 30 minutes later.

Inverter (Master)			LCD Module			Inverter (Slavor)
	Ⓐ Ⓐ	1 2	HV (White +) / HV(Pink +)			
	Ⓐ Ⓐ	1 2	HV (White -) / HV(Pink -)			
	Ⓐ Ⓐ	1 2	HV (White +) / HV(Pink +)			
	Ⓐ Ⓐ	1 2	HV (White -) / HV(Pink -)			
	Ⓐ Ⓐ	1 2	HV (White +) / HV(Pink +)			
	Ⓐ Ⓐ	1 2	HV (White -) / HV(Pink -)			
	Ⓐ Ⓐ	1 2	HV (White +) / HV(Pink +)			
	Ⓐ Ⓐ	1 2	HV (White -) / HV (Pink -)			

HV (Pink -) / HV (White -)	1 2	Ⓐ Ⓐ
HV (Pink +) / HV (White +)	1 2	Ⓐ Ⓐ
HV (Pink -) / HV (White -)	1 2	Ⓐ Ⓐ
HV (Pink +) / HV (White +)	1 2	Ⓐ Ⓐ
HV (Pink -) / HV (White -)	1 2	Ⓐ Ⓐ
HV (Pink +) / HV (White +)	1 2	Ⓐ Ⓐ
HV (Pink -) / HV (White -)	1 2	Ⓐ Ⓐ
HV (Pink +) / HV (White +)	1 2	Ⓐ Ⓐ

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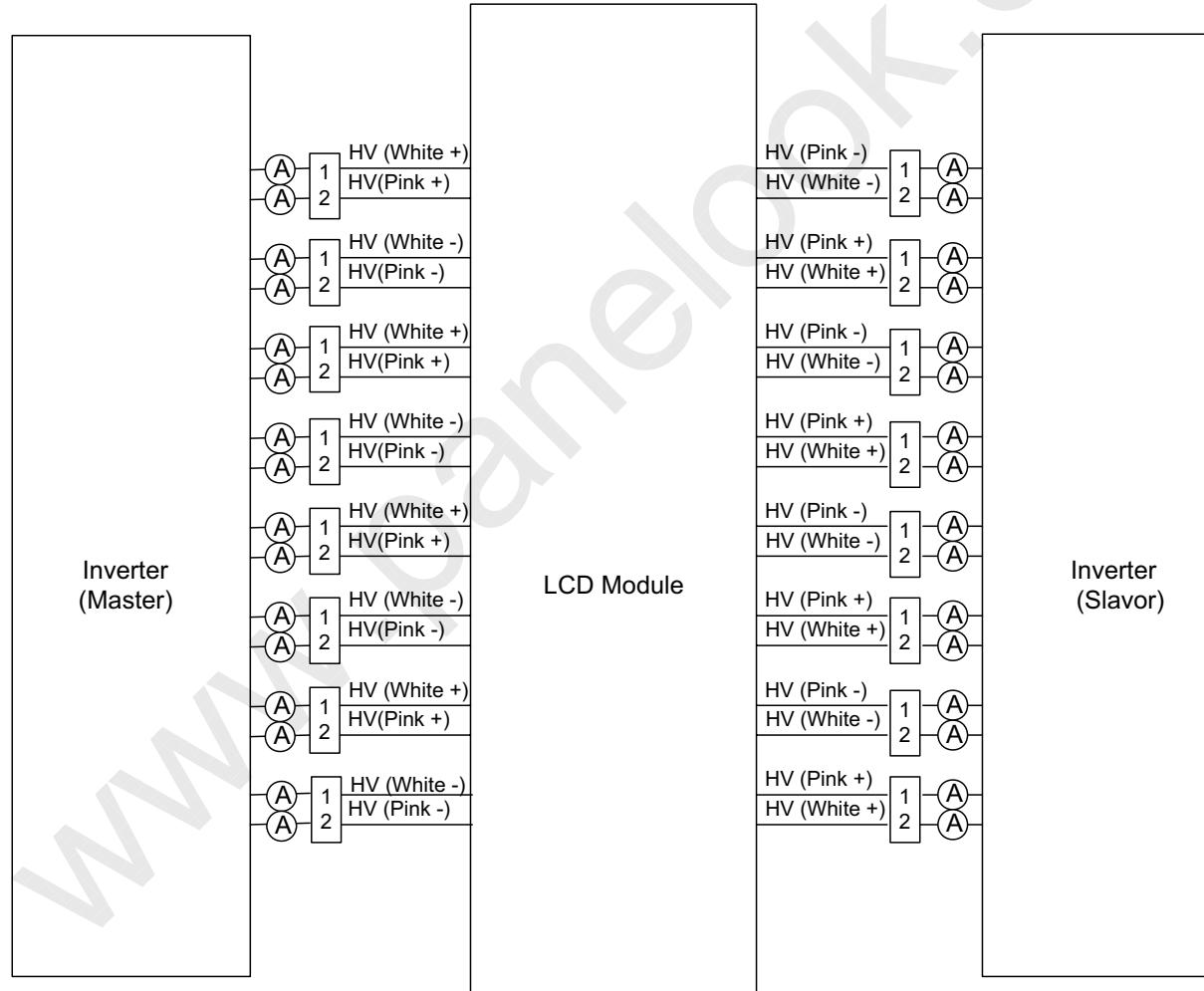
3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	3.15	3.3	3.45	V	maximum duty ratio
	MIN			—	0	—	V	minimum duty ratio
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
VBL Rising Time		Tr1	—	30	—	50	ms	
VBL Falling Time		Tf1	—	30	—	50	ms	
PWM Delay Time		TPWM	—	100	—	300	mS	
Input impedance		RIN	—	1	—	—	MΩ	
BLON Delay Time		Ton	—	1	—	—	ms	
BLON Off Time		Toff	—	1	—	—	ms	

Note (1) The power sequence and control signal timing are shown in the following figure.

Note (2) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

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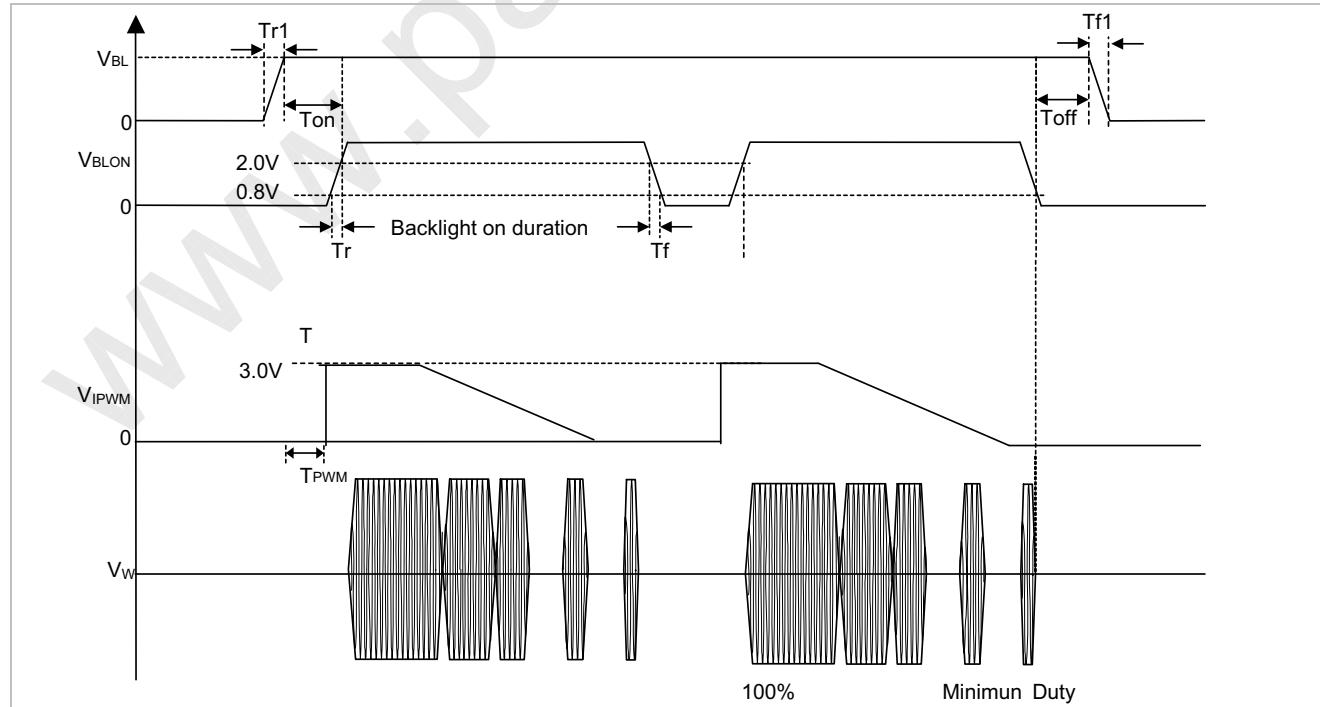
4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE

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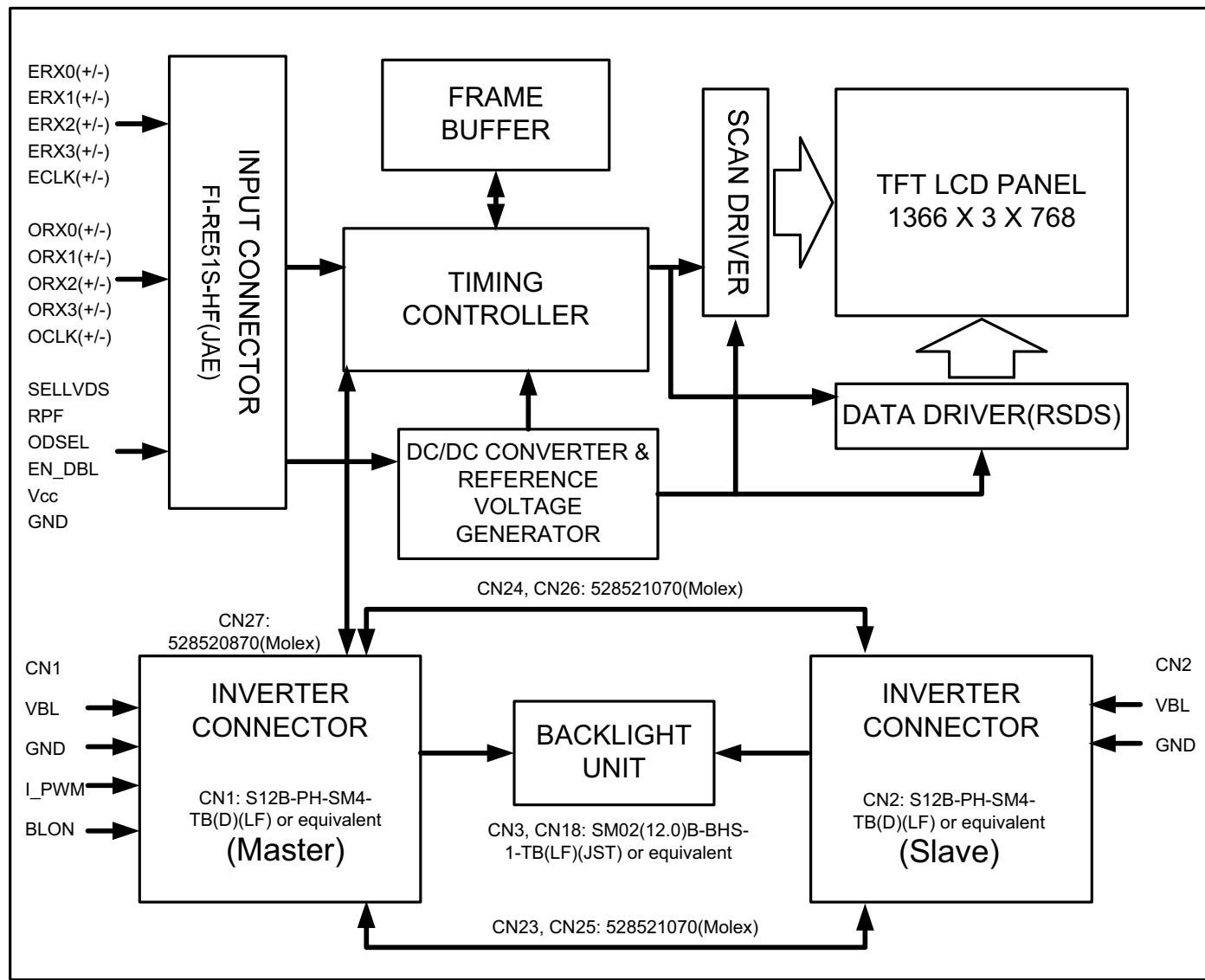
5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

Pin	Name	Description	Note
1	N.C.	No Connection	(2)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	Low : VESA Format (Default), High : JEIDA Format	(3)
8	RPF	Display Rotation	(4)
9	ODSEL	Overdrive Lookup Table Selection	(5)
10	EN_DBL	Dynamic BLU Enable	(6)
11	Reserved	Reserved	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input.	
20	ECLK+	Even pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	Odd pixel Negative LVDS differential clock input.	
36	OCLK+	Odd pixel Positive LVDS differential clock input.	

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37	GND	Ground	
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	N.C.	No Connection	(2)
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	GND	Ground	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Connector part No: FI-RE51S-HF (JAE) or equivalent.

Note (2) Reserved for internal use. Please leave it open.

Note (3) Low : VESA LVDS Format (default), High : JEIDA LVDS Format.

Note (4) Low : normal display (default), High : display with 180 degree rotation.

CMI MEI   CMI MEI

Normal Display   180º Rotation Display

Note (5) Overdrive lookup table selection. The overdrive lookup table shoule be selected in accordance with the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table optimized for 120Hz frame rate
H	Lookup table optimized for 100Hz frame rate

Note (6) Low : function disabled (default), High : Dynamic Backlight function enable.

Note (7) Low = Open or Connect to GND, High = Connecto to +3.3V

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5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN3-CN22: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST. The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF).

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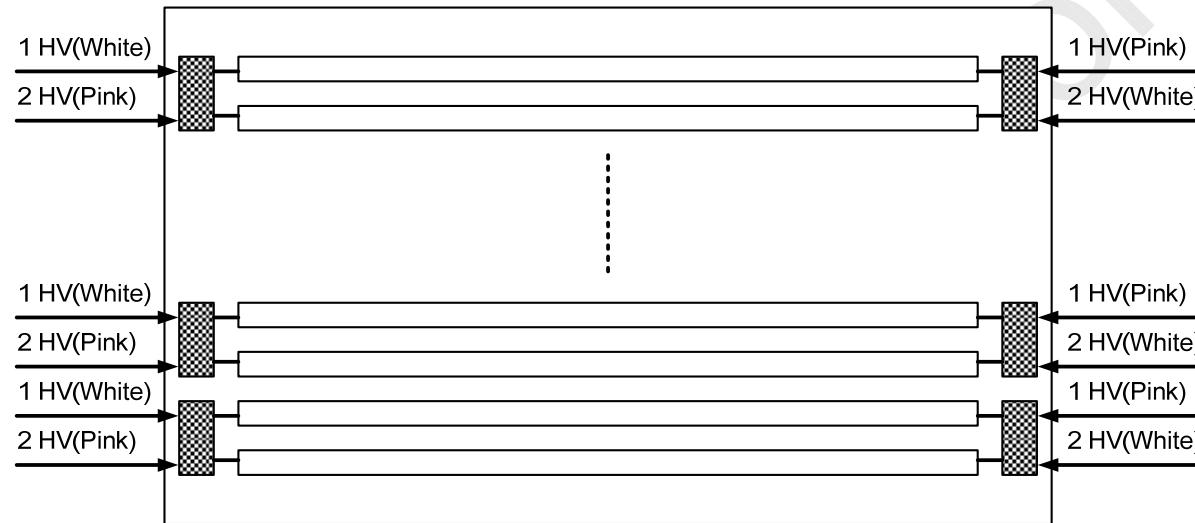
5.3 INVERTER UNIT

CN1: S12B-PH-SM4-TB(D)(LF)(JST) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	I_PWM	Internal PWM Control Signal
12	BLON	BL ON/OFF

CN2: S12B-PH-SM4-TB(D)(LF)(JST) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN3-CN18: SM02(12.0)B-BHS-1-TB(LF)(JST) or equivalent

Pin №	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

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CN23-CN26: 528521070 (Molex)

Pin №	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

CN27: 528520870 (Molex)

Pin №	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board

Note (1) Floating of any control signal is not allowed.

5.4 BLOCK DIAGRAM OF INTERFACE

TxIN

ER0 – ER7
EG0 – EG7
EB0 – EB7
DE

OR0 – OR7
OG0 – OG7
OB0 – OB7
DCLK

Host
Graphic
Controller

LVDS Transmitter
THC63LVDM83A
(LVDF83A)

ERx0 +
ERx0 -
ERx1 +
ERx1 -
ERx2 +
ERx2 -
ERx3 +
ERx3 -
ECLK +
ECLK -
ORx0 +
ORx0 -
ORx1 +
ORx1 -
ORx2 +
ORx2 -
ORx3 +
ORx3 -
OCLK +
OCLK -

PLL

RxOUT

ER0 – ER7
EG0 – EG7
EB0 – EB7
DE

OR0 – OR7
OG0 – OG7
OB0 – OB7
DCLK

DCLK
Timing
Controller

LVDS Receiver

51Ω　$100pF$

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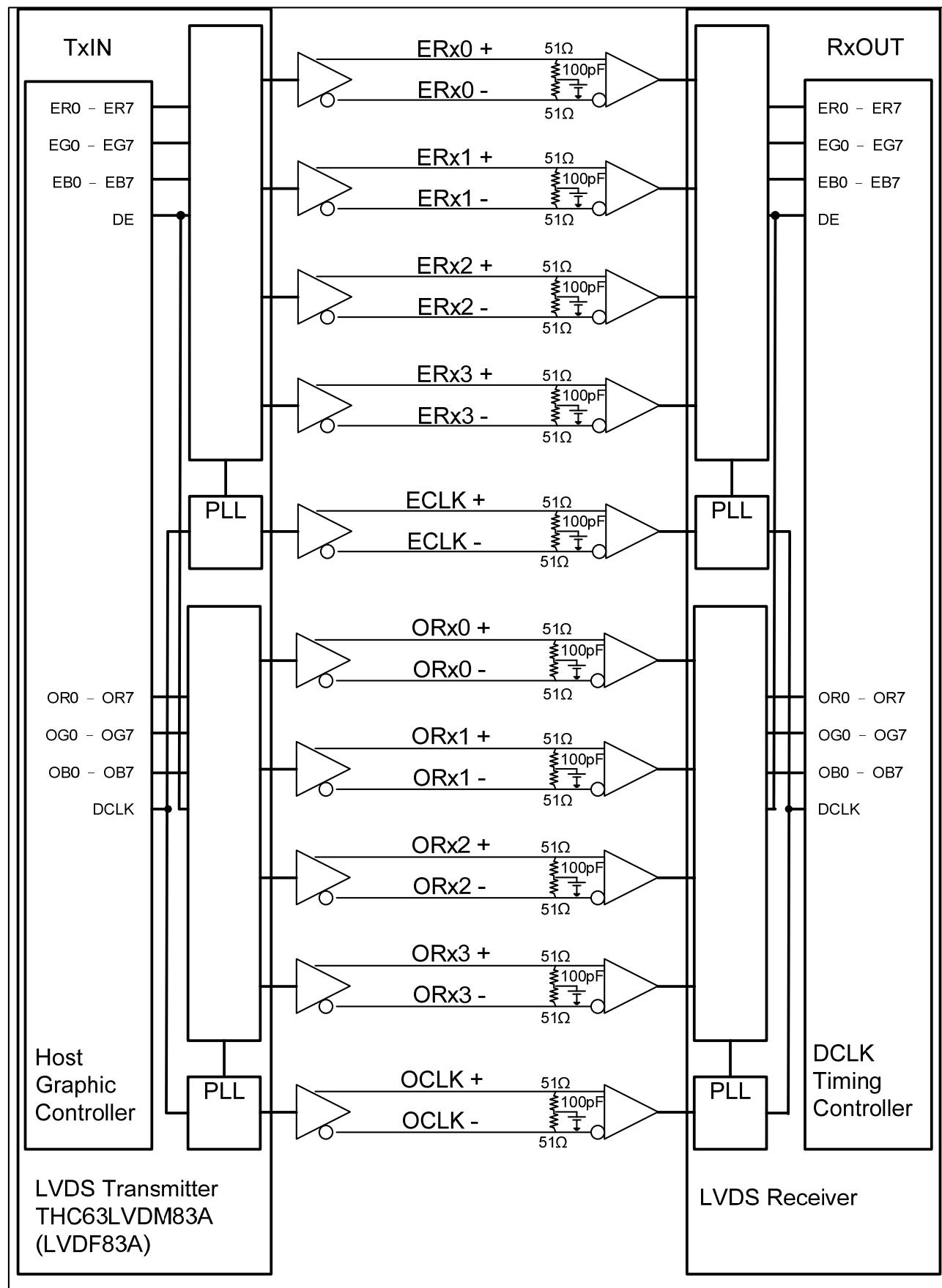
ER0~ER7: Even Pixel R data

EG0~EG7: Even Pixel G data

EB0~EB7: Even Pixel B data

OR0~OR7: Odd Pixel R data

OG0~OG7: Odd Pixel G data

OB0~OB7: Odd Pixel B data

DE: Data enable signal

DCLK: Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Note (3) Two pixel data sent into module for every clock cycle. The first pixel of frame is even pixel and the second pixel is odd pixel

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5.5 LVDS INTERFACE

SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
LVDS_SEL =L or OPEN	LVDS_SEL = H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	LVDS_SEL =L or OPEN	LVDS_SEL = H
R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
DCLK		31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE　: Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

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5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red Gray Scale	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green Gray Scale	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue Gray Scale	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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## 6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	56	76	82	MHZ	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate		94	100	106	Hz	(1)
			114	120	126	Hz	(1)
	Total	Tv	778	795	888	Th	Tv=Tvd+Tvb
	Display	Tvd	768	768	768	Th	-
	Blank	Tvb	10	27	120	Th	-
Horizontal Active Display Term	Total	Th	762	899	968	Tc	Th=Thd+Thb
	Display	Thd	683	683	683	Tc	-
	Blank	Thb	79	216	285	Tc	-

Note(1) : (ODSEL) = (L), (H). Please refer to 5.1 for detail information.

Note(2) : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM

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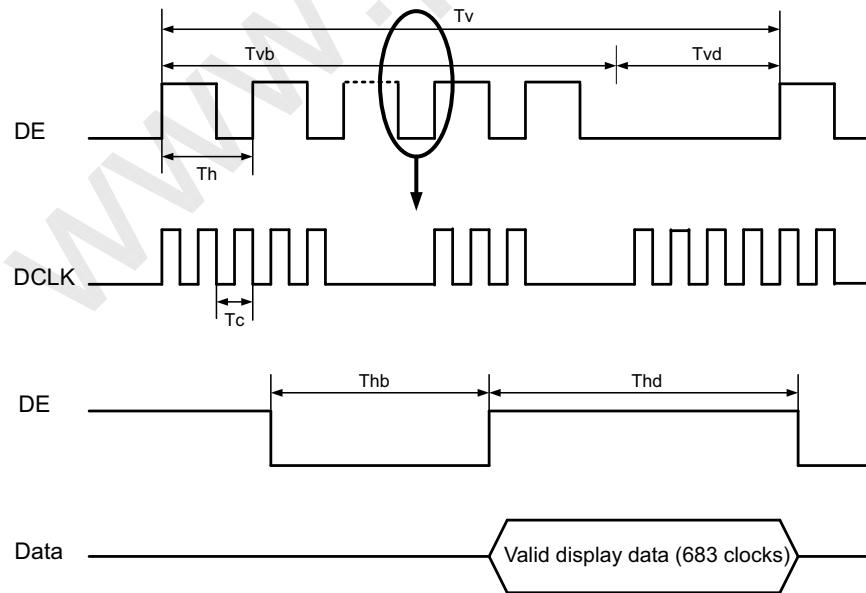
LVDS INPUT INTERFACE TIMING DIAGRAM

Tc

RXCLK +

RXn +/-

TIvsu TIvhd

$\frac{1T}{14}$ $\frac{3T}{14}$ $\frac{5T}{14}$ $\frac{7T}{14}$ $\frac{9T}{14}$ $\frac{11T}{14}$ $\frac{13T}{14}$
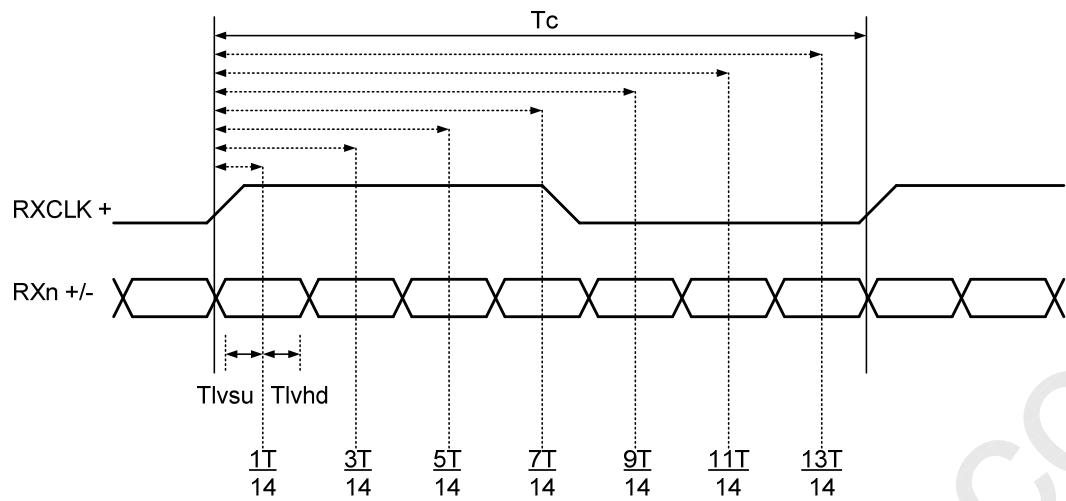
6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.

POWER ON/OFF SEQUENCE
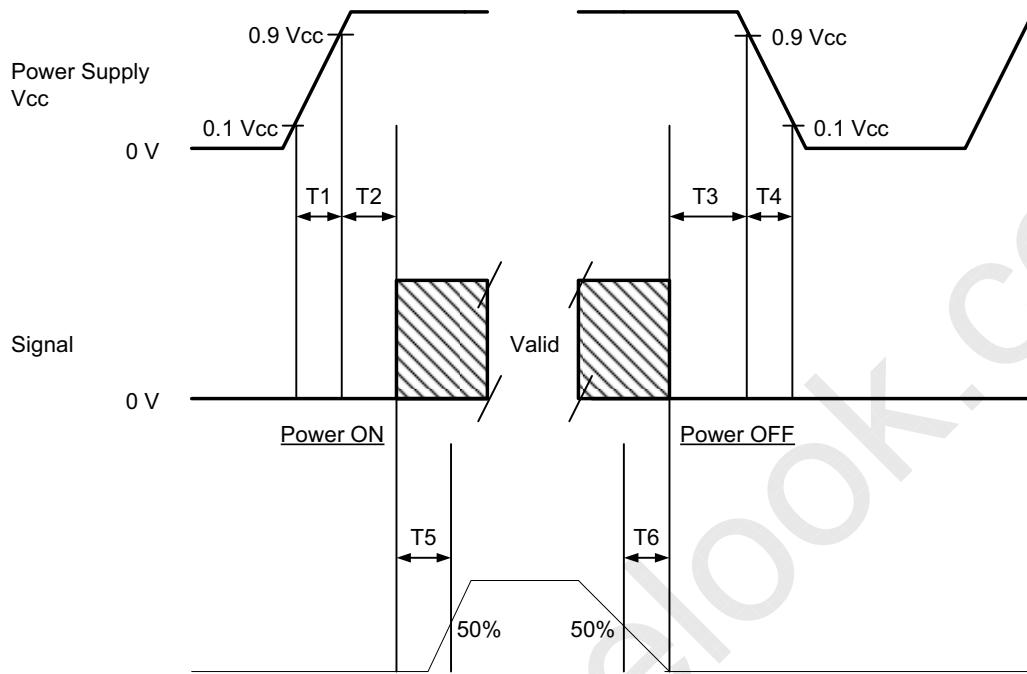
Signal	Min.	Typ.	Max.	Unit	Note
T1	0.5	-	10	ms	-
T2	0	-	50	ms	-
T3	0	-	50	ms	-
T4	500	-	-	ms	-
T5	500	-	-	ms	-
T6	100	-	-	ms	-

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

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7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	6.5±0.5	mA
Oscillating Frequency (Inverter)	FW	50±3	KHz
Vertical Frame Rate	Fr	120	Hz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		1200	1500	-	-	Note (2)
		Dynamic CR		-	6000	-		
Response Time		Gray to gray		-	4.0	8.0	ms	Note (3)
Center Luminance of White		LC		400	500	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.3	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx	θx=0°, θy =0° Viewing angle at normal direction	Typ. -0.03	0.643	Typ. +0.03	-	Note (6)
		Ry			0.332		-	
	Green	Gx			0.268		-	
		Gy			0.589		-	
	Blue	Bx			0.143		-	
		By			0.066		-	
	White	Wx			0.280		-	
		Wy			0.285		-	
	Color Gamut	C.G		68	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	Note (1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

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Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R

Normal

θ x =θ y = 0º

θy-   θy+

θX- = 90º   x-

12 o'clock direction
θy+ = 90º

θx-   y+
θx+

6 o'clock   y-
θy- = 90º

x+   θX+ = 90º
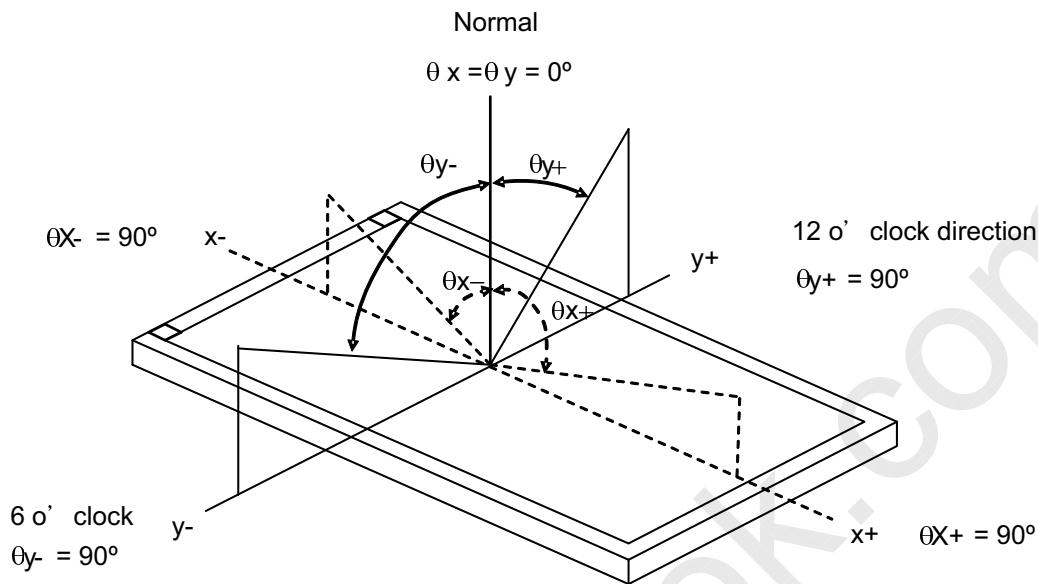
Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

The measured value will be "Dynamic CR" only when the function of dynamic contrast ratio is enabled.

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response

100 %
90 %

10 %
0 %

Time

Gray to Gray
Switching Time

Gray to Gray
Switching Time

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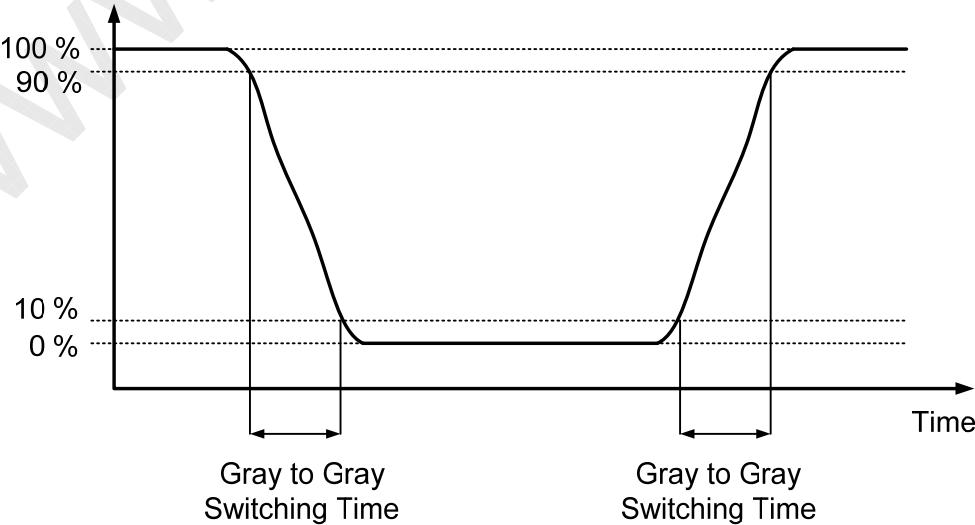
The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0, 63,127,191,255 to each other.

Note (4) Definition of Luminance of White (LC, LAVE):

Measure the luminance of gray level 255 at center point and 5 points

LC = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

CT = | YB − YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)

Active Area

(0,0)

$Y_{A,U}$(D/2,W/8)

$Y_{A,L}$(D/8,W/2)   Gray 128 $Y_{A,R}$(7D/8,W/2)

$Y_{A,D}$(D/2,7W/8)

Active Area

(0,0)

$Y_{B,U}$(D/2,W/8)

(D/4,W/4)

$Y_{B,L}$(D/8,W/2)   Gray 0 $Y_{B,R}$(7D/8,W/2)

$Y_{B,D}$(D/2,7W/8)
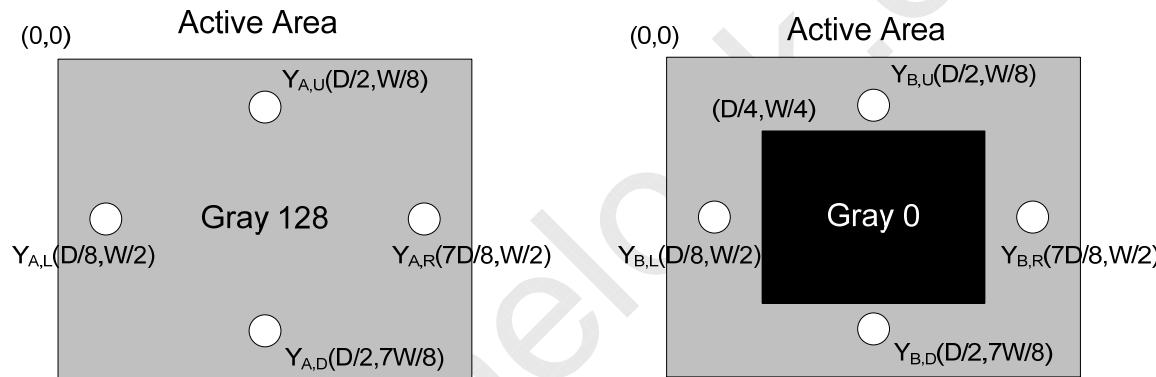
Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.

LCD Module

LCD Panel

Center of the Screen   Display Color Analyzer

(Minolta CA210)

Light Shield Room

(Ambient Luminance < 2 lux)

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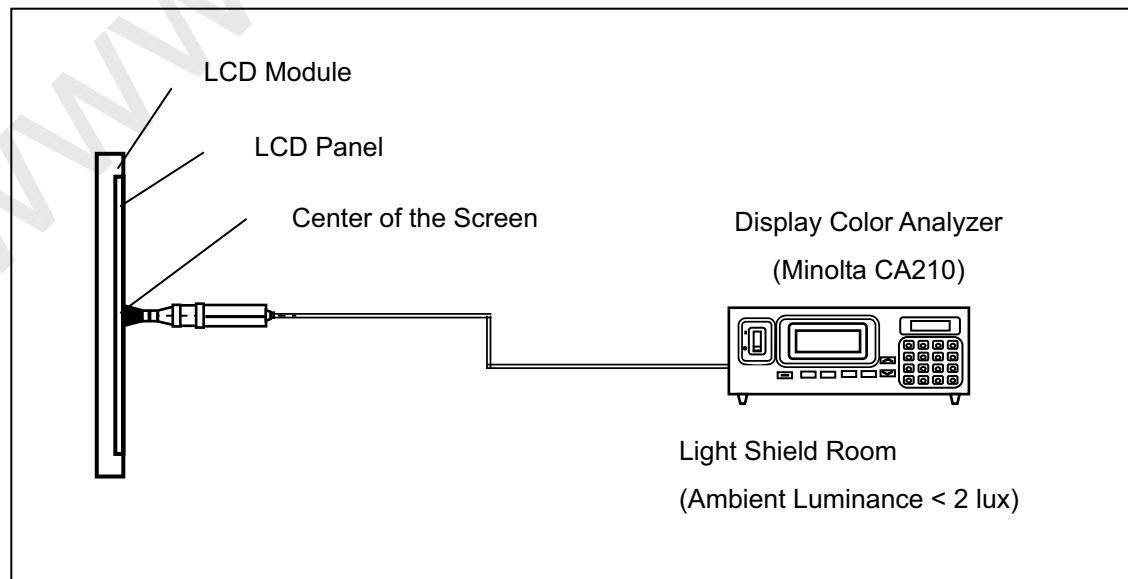
Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

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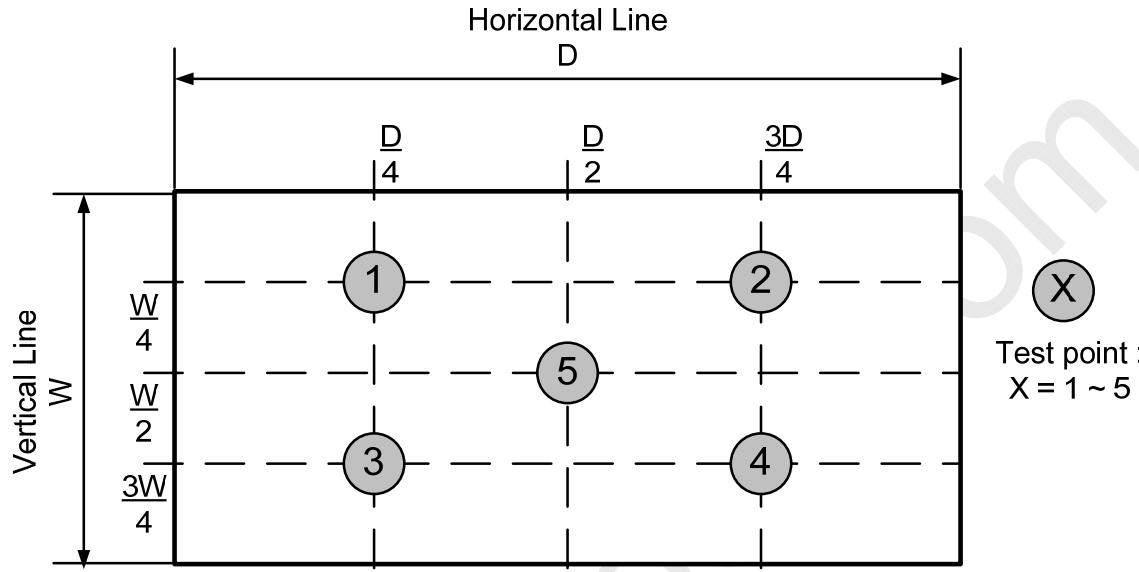
8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1]   Do not apply rough force such as bending or twisting to the module during assembly.

[2]   It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3]   Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4]   Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5]   Do not plug in or pull out the I/F connector while the module is in operation.

[6]   Do not disassemble the module.

[7]   Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8]   Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9]   When storing modules as spares for a long time, the following precaution is necessary.

    [9.1]   Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

    [9.2]   The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10]   When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1]   The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2]   If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3]   After the module's end of life, it is not harmful in case of normal operation and storage.

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9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.
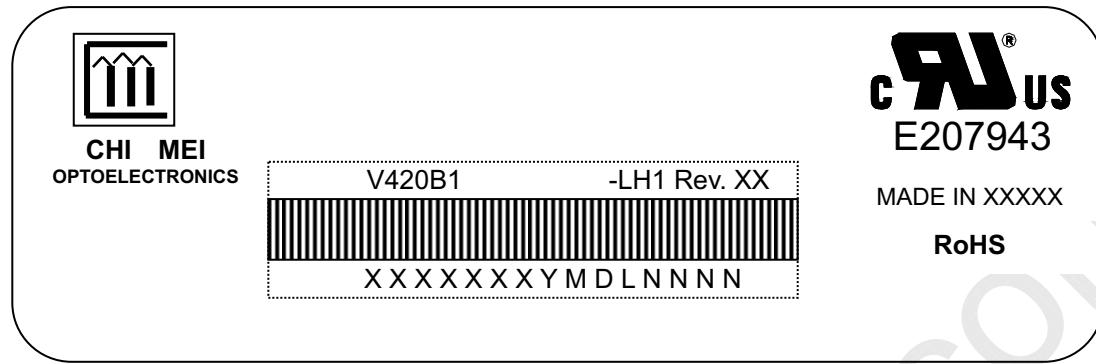
Model Name: V420B1-LH1

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X X Y M D L N N N N
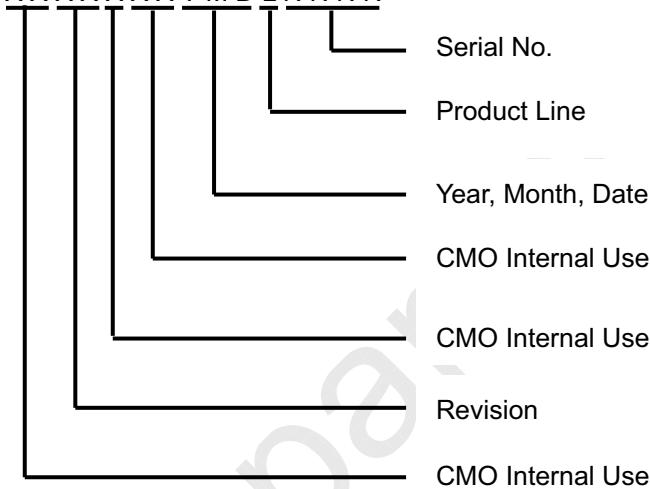
Serial ID includes the information as below:

Manufactured Date:

        Year: 0~9, for 2000~2009

        Month: 1~9, A~C, for Jan. ~ Dec.

        Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

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10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

3 LCD TV modules / 1 Box

Box dimensions: 1080(L) X 282 (W) X 685(H)

Weight: approximately 45Kg (3 modules per box)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method.
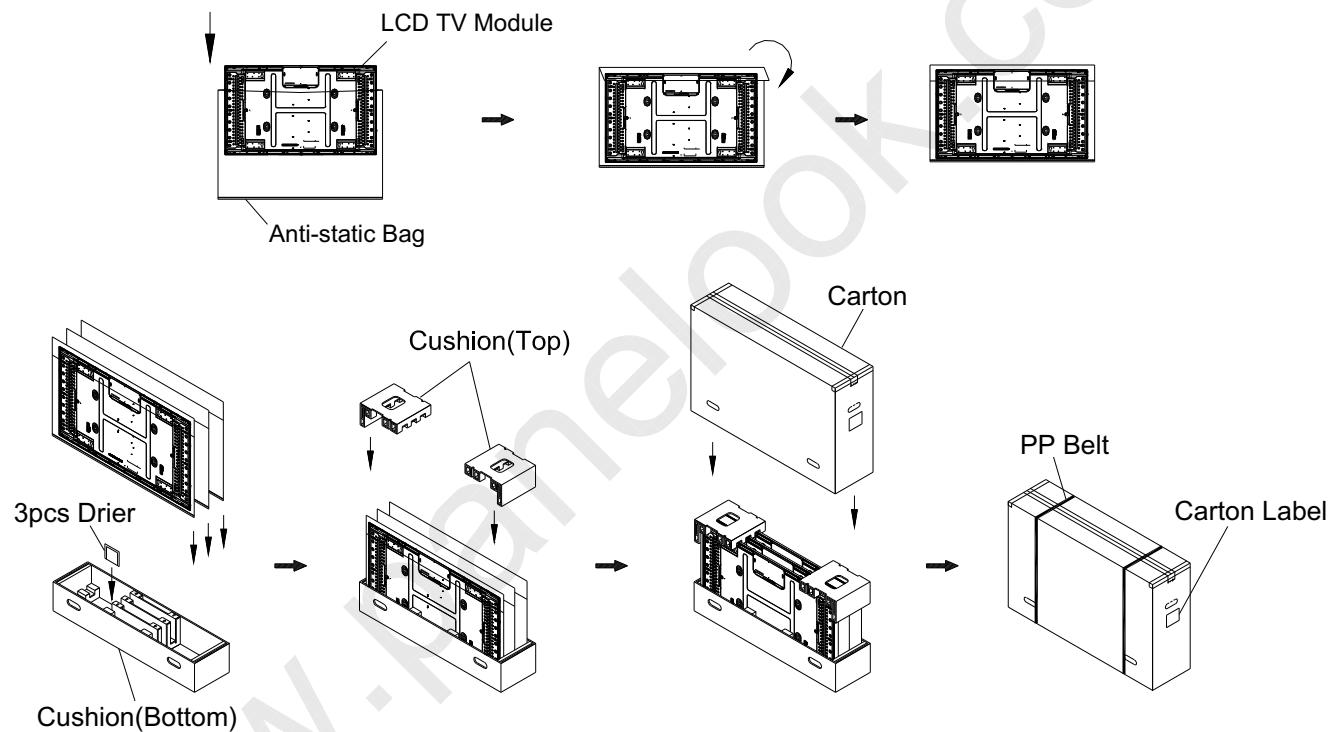
Figure.10-1 packing method

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Sea / Land Transportation (40ft HQ Container)
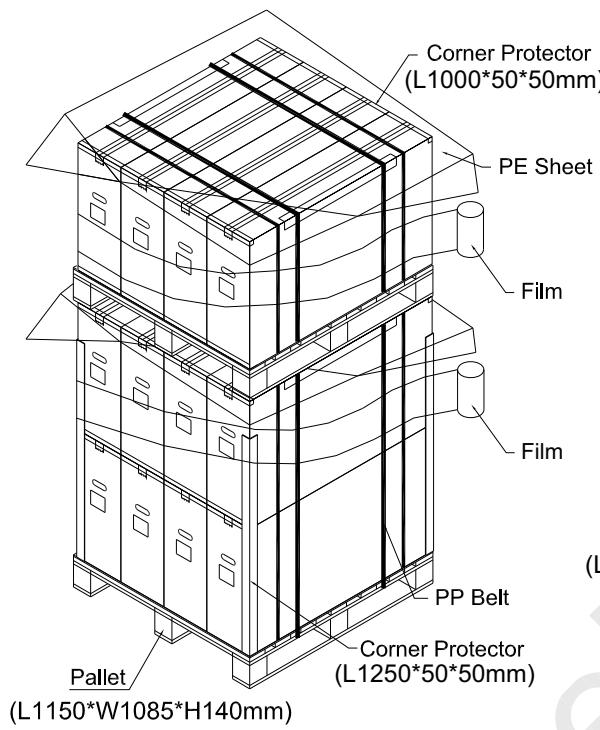
Air Transportation &
Sea / Land Transportation (40ft Container)
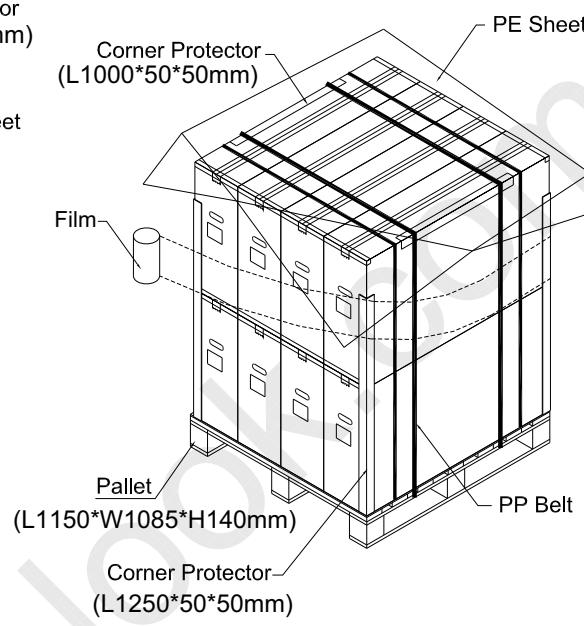
Figure.10-2 Packing method

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11. MECHANICAL CHARACTERISTICS
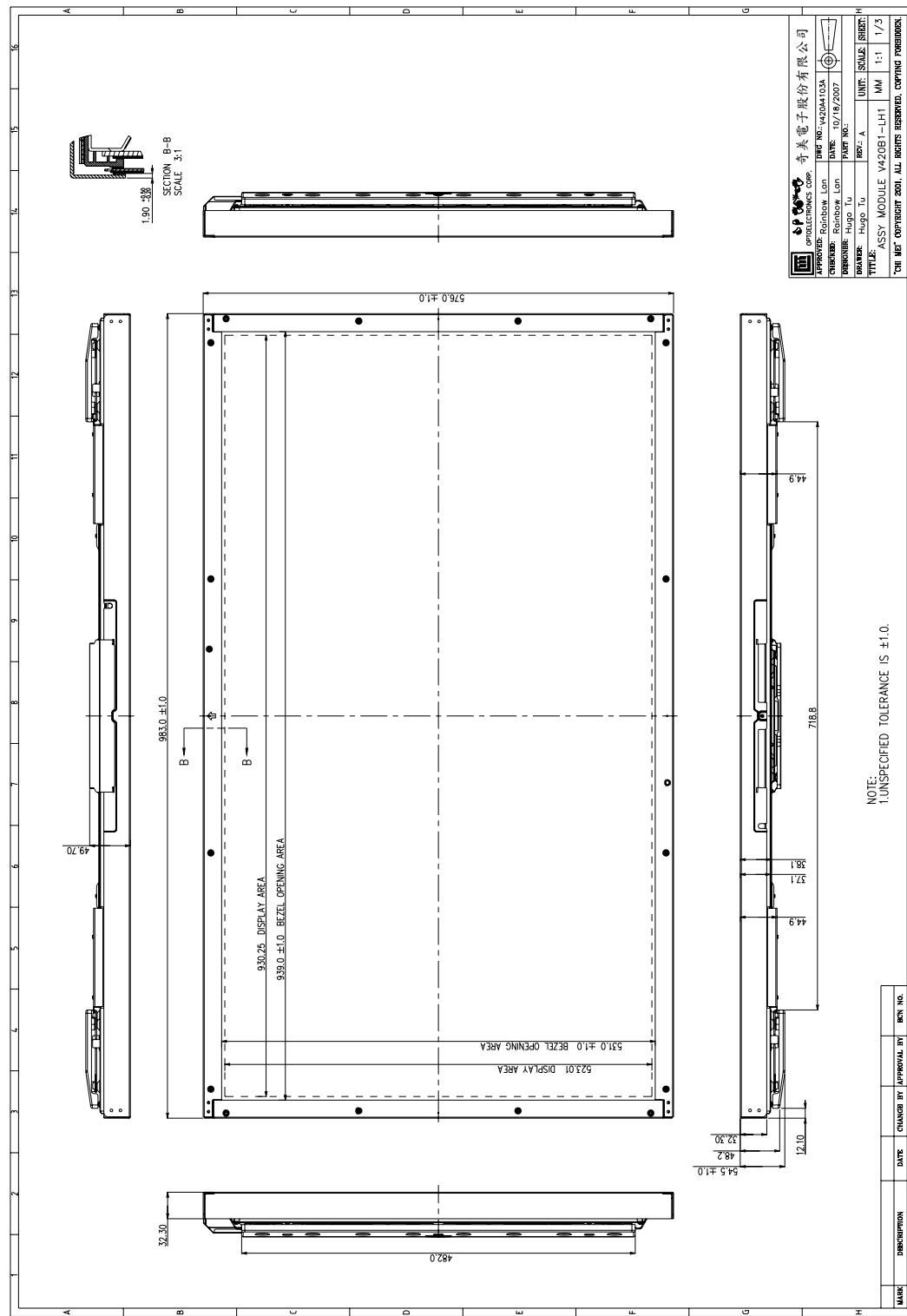
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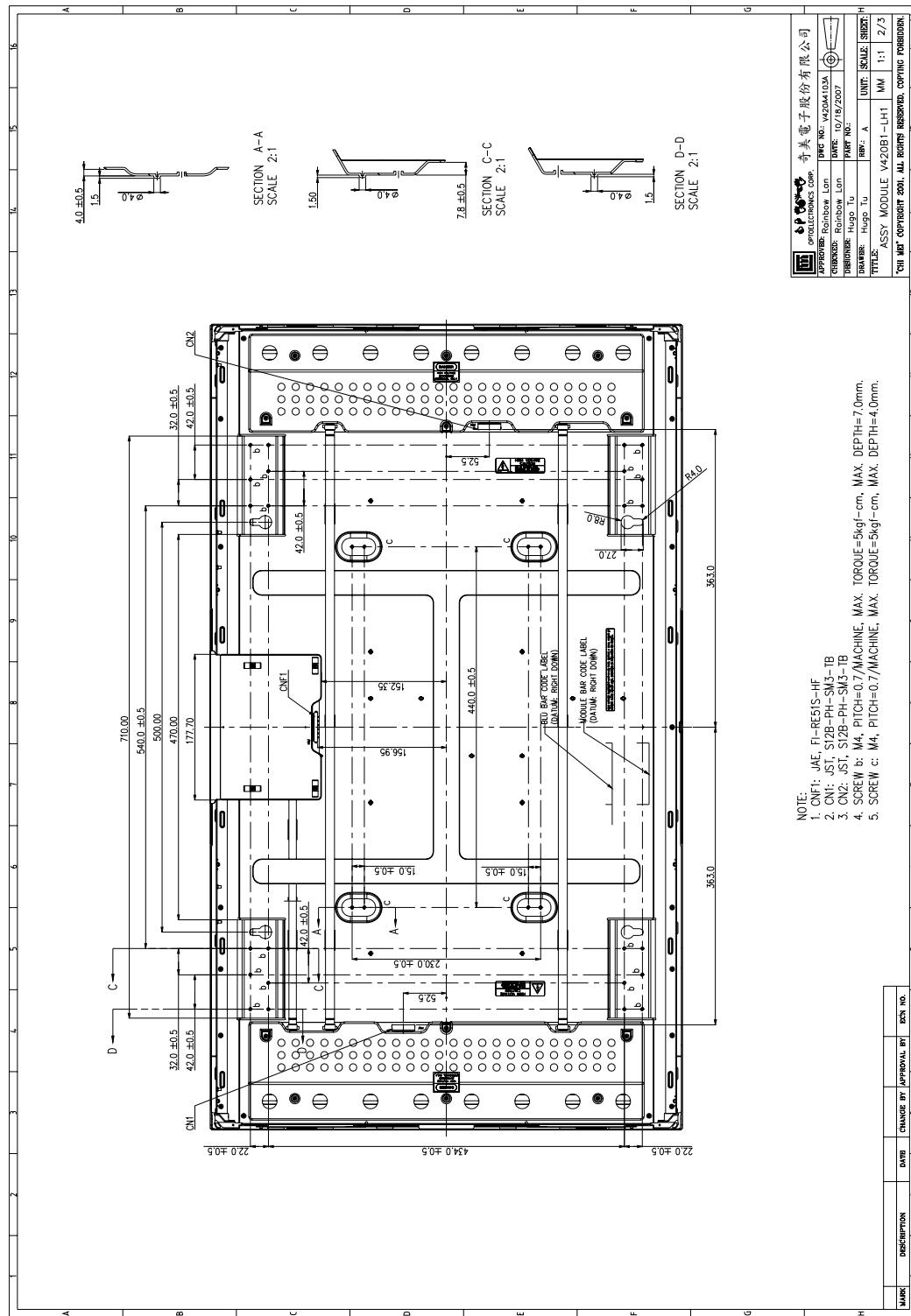
Issue Date:Oct.19.2007
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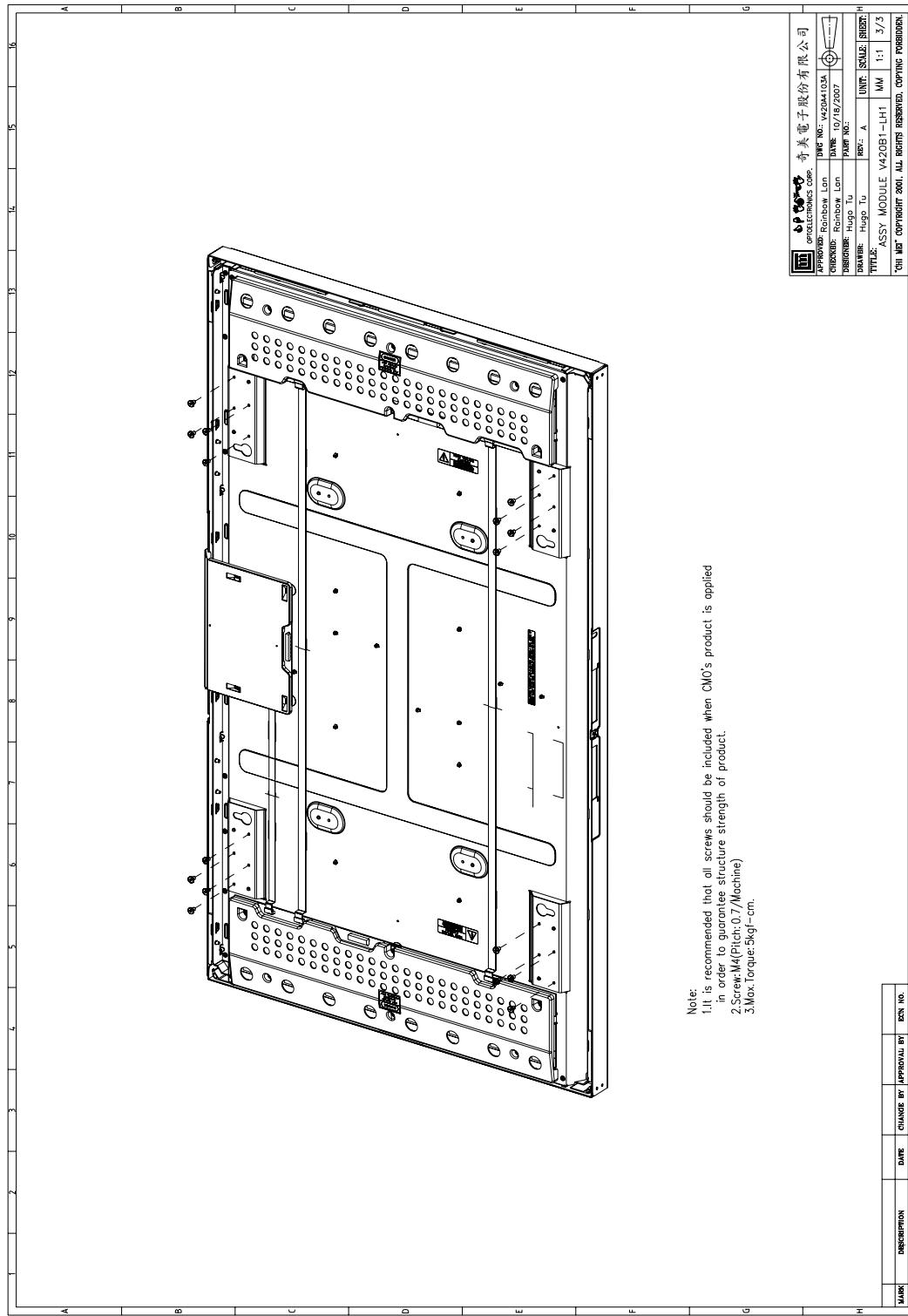
Note:
1.It is recommended that all screws should be included when CMO's product is applied in order to guarantee structure strength of product.
2.Screw:M4(Pitch:0.7/Machine)
3.Max.Torque:5kgf-cm.

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